21. A circuit as claimed in claim 19, for additionally deriving a fifth order signal from an input signal, wherein the input circuitry provides the input signal along fourth and fifth paths, and further comprises a third combiner for combining the input signal from the fourth path with the third order signal to produce a fourth order signal, and a fourth combiner for combining the input signal from the fifth path with the fourth order signal to produce a fifth order signal.

22. A circuit as claimed in claim 19, wherein the input signal is a radio frequency signal.

23. A circuit as claimed in claim 19, further comprising an injector for injecting a direct current signal into at least one of the signal paths.

24. A circuit as claimed in claim 23, wherein the injector is arranged to inject the direct current signal into the squared signal path for adding to the second order signal to cancel input signal energy in the third order signal.

25. A circuit as claimed in claim 24, further comprising an error corrector arranged to compare the third order signal with the input signal to produce an error correction signal for controlling the injection of the direct current signal into the squared signal path.

26. A circuit as claimed in claim 25, wherein the error corrector is arranged to translate the frequency of the third order signal by an oscillator signal prior to correlation with the input signal to produce a correlation signal which is processed in a digital signal processor by comparison with the oscillator signal to produce the error correction signal.

27. A circuit as claimed in claim 23, further comprising an injector for injecting the direct current signal into the second squared signal path for adding to the second order signal to cancel input signal energy and third order signal energy in the fifth order signal.

28. A circuit as claimed in claim 25, further comprising an error corrector arranged to compare the fifth order signal with the third order signal to produce an error correction signal for controlling the injection of the direct current signal into the second squared signal path.

29. A circuit as claimed in claim 19, wherein the combiners are selected from mixers and multipliers.

30. A circuit as claimed in claim 19, wherein the input circuitry comprises at least one splitter for providing the input signal along the signal paths.

31. A circuit as claimed in claim 19, wherein the input circuitry comprises at least one directional coupler for providing the input signal along the signal paths.

32. A polynomial predistorter including a circuit for deriving a third order predistortion signal from an input signal, comprising input circuitry for providing an input signal to the circuit along first, second and third paths, a first combiner for combining the input signal from the first and the second paths to produce a second order signal on a squared signal path, a filter for low-pass filtering the second order signal to remove components at the frequency of the input signal and harmonics thereof, and a second combiner for combining the filtered second order signal from the squared signal path with the input signal from the third path to produce a third order signal.

33. A method of deriving a third order predistortion signal from an input signal, comprising providing an input signal to a circuit along first, second and third paths, combining the input signal from the first and second paths to produce a second order signal on a squared signal path, low-pass filtering the second order signal to remove components at the frequency of the input signal and harmonics thereof, and combining the filtered second order signal from the squared signal path with the input signal from the third path to produce a third order signal.

34. A circuit as claimed in claim 19, further comprising a generator for creating at least one further, different, odd-order signal, each said distinct, further odd-order signal being created by combining the input signal with itself.

35. A polynomial predistorter according to claim 32, further comprising a generator for creating at least one further, different, odd-order signal, each said distinct, further odd-order signal being created by combining the input signal with itself.

A1

36. A method according to claim 33, further comprising creating at least one further, different, odd-order signal, each said distinct, further odd-order signal being created by combining the input signal with itself.

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